Spin Transport & Scattering in Ferromagnetic Semiconductor Heterostructures
Outline

- Controlling spins in semiconductor heterostructures: overview
- Spin transport & scattering in (Ga,Mn)As devices:
  - Non-collinear spin valve effect in trilayer devices (Xiang et al, in preparation)
  - Pinning and controlling domain walls at constrictions & interfaces (Eid et al, in preparation)
- Interfacial control of ferromagnetism in (Ga,Mn)As
  - Exchange biasing of (Ga,Mn)As by MnO (Eid et al., APL 85, 1556 [2004], Eid et al. J. Appl. Phys. 97, 10D304 [2005])
  - Nanoengineered $T_c$ in submicron (Ga,Mn)As wires (Eid et al, APL 86, 152505 [2005])
Epitaxial integration and patterning of magnetic materials with established growth/processing protocols

- paramagnetic semiconductors
- ferromagnetic semiconductors
- ferromagnetic metals
- antiferromagnets

GaAlAs/ZnSe/(Zn,Cd,Mn)Se 2DEG Cantilevers

II-VI microdisk on ~100nm diameter AlGaAs pedestal

100 nm

Submicron (Ga,Mn)As device For domain wall pinning
Towards Semiconductor Spintronics - I

Create, control & detect spin polarization of electrons/holes in semiconductors
- Electric fields
- Exchange interactions

Electrically controlled spin dynamics

4x1/8 ml MnSe

Change overlap between electrons and Mn via electrical bias

Parabolic potential using (Zn,Cd)Se "digital alloy"; Mn ions in center.

Myers et al, PRB 72, 041302(R) [2005]
Towards Semiconductor Spintronics - II

Create, control & detect spin polarization of electrons/holes in semiconductors
- Electric fields
- Exchange interactions
- Circularly polarized photons

Q-factor engineering of electron spin coherence in GaAs/GaAlAs microdisk lasers

Towards Semiconductor Spintronics -- III

Exploit spin transport in both conventional and magnetic semiconductors
• Spin injection & spin polarized transport
• Spin Hall effect
• Unipolar spin diodes & transistors (Flatte & Vignale)
• Magnetic bipolar transistors (Flatte et al, Zutic et al)

Need to control:
• Switching field of different device elements via
  • Shape anisotropy
  • Magneto-crystalline anisotropy, strain
  • Exchange bias
• Domain wall locations
  • Pinned: fixed architecture
  • Moveable: reconfigurable (Holleitner et al., 2004, Yamounichi et al. 2004)
Ga$_{1-x}$Mn$_x$As: the “canonical” ferromagnetic semiconductor

- Hole-mediated ferromagnetism: Mn$^{2+}$ ($S = 5/2$) in zinc-blende GaAs lattice
- Low temperature MBE: Mn interstitial & As antisite defects (donors)
- Post-growth annealing: Mn interstitials to free surface of sample [Yu et al., PRB (2002), Edmonds et al, PRL (2004)]
- $T_C$ can be increased up to $\sim$170 K. ($\sim$240 K? Tanaka)
- Origin of ferromagnetism: impurity band (e.g, Burch et al, 2006)
Annealing Effects are Suppressed in Heterostructures!


See also: Chiba et al, APL (2003)

- Capping (Ga,Mn)As with a thin epitaxial layer of GaAs suppresses beneficial aspects of annealing
- Diffusing interstitials (donors) create pn junction at interface
I. Non-collinear spin valve effect in ferromagnetic semiconductor trilayer devices

With G. Xiang, M. Zhu, B. L. Sheu, & P. Schiffer (in preparation)
Searching for the spin valve effect in (Ga,Mn)As devices

In (Ga,Mn)As:
- Short hole spin diffusion length (~few nm)
- Short elastic mean free path (<2 nm)
- Strong magnetoresistance (anisotropic magnetoresistance, anomalous Hall effect, planar Hall effect)

\[
\frac{\Delta R}{R} = \frac{(\alpha - 1)^2}{4(\alpha + p d_{\text{NM}} / d_{\text{FM}})(1 + p d_{\text{NM}} / d_{\text{FM}})}
\]

**Key Factors:**
- \( \alpha = \rho_\downarrow / \rho_\uparrow \)
- \( p = \rho_{\text{NM}} / \rho_\uparrow \)
- \( d_{\text{NM}} / d_{\text{FM}} \)
Spin Valve Effect in Ferromagnetic Semiconductor Trilayers

- Trilayer devices wherein ferromagnetic layers & spacer layer have comparable conductivity
- Annealing creates distinct $H_C$ for upper/lower GaMnAs layers
- Speculate that annealing also produces spin-dependent scattering at interfaces
- Spacer thickness varied: 2 nm, 5 nm & 10 nm
- Annealing time varied for 5 nm spacer
Spin Valve Effect in Ferromagnetic Semiconductor Trilayers

- **Planar Hall effect** tracks magnetization orientation: magnetization of each layer switches by $90^0$
- Comparison between PHE and MR shows non-collinear spin valve effect: enhanced resistance for orthogonal magnetization orientation
- Unusual “structure” due to interplay between AMR and spin valve effect

(Xiang *et al.*, in preparation)
Magnetoresistance in trilayers: spacer thickness dependence

All devices annealed at 190°C for 1 hr

- Sample A (2nm spacer) MR similar to single FM layer’s
- Sample B (5nm spacer) MR \( \rightarrow \) positive \( \Delta R \)
- Sample C (10nm spacer) MR looks like addition of two FMs

\[ T = 4.2 \text{ K} \]
II. Pinning, measuring and controlling domain walls in patterned (Ga,Mn)As devices

With **K. F. Eid**, G. Xiang, A. Balk, B. L. Sheu, O. Maksimov, & P. Schiffer

(in preparation)
Pinning & detecting domain walls in (Ga,Mn)As

Submicron (Ga,Mn)As device for domain wall pinning

30 nm GaMnAs
1μm GaInAs
GaAs substrate

GaMnAs
InGaAs
GaAs substrate

A
B
C
D
E
F

100 nm

Graphs showing changes in resistance with applied magnetic field (H) for different contact configurations (AD, BE, FC).
Pinning & detecting domain walls in (Ga,Mn)As

Submicron (Ga,Mn)As device for domain wall pinning

- Circulating currents in vicinity of pinned DW
- Longitudinal MR is antisymmetric in magnetic field due to $R_{xy}$ (anomalous Hall effect) contribution to $R_{xx}$
- Note: intrinsic DW resistance negligible (Chiba et al 2006, Tang et al 2004)
Electrically manipulating domain walls in (Ga,Mn)As devices

- Lateral channel size: 20 μm; middle element: 40 μm long
- Vertical etching steps define (Ga,Mn)As elements with different coercivity (Yamounichi et al, Science 2004)
- Current pulses of 100 ms width sent in alternating “up” & “down” sequence at 20 s intervals
- Monitor switching of middle element via anomalous Hall effect
- Note: DW motion is opposite to direction of current pulse
Electrically manipulating domain walls in (Ga,Mn)As devices

- Typical current density required to completely switch middle element (at 70 K) $\sim 2 \times 10^4$ A/cm$^2$
- Caveat: details of switching threshold very dependent on device processing, thermal history, etc.
- Often find different threshold current density depending on initial state
- Caveat: details of switching threshold very dependent on device processing, thermal history, etc.
III. Exchange biasing of (Ga,Mn)As

With K. F. Eid, M. B. Stone, K. C. Ku, O. Maksimov
T. Shih, C. Palmstrom & P. Schiffer
Appl. Phys. Lett. 85, 1556 [2004]
J. Appl. Phys. 97, 10D304 [2005]
Exchange Biasing

- Meikeljohn (1956): unidirectional anisotropy when FM/AF bilayer ($T_N < T_C$) is field cooled from $T < T_C$ to $T < T_B < T_N$
- Magnetization hysteresis loop shifts in direction opposite to cooling field & widens below “blocking temperature” ($T_B$)
- Critical for spintronic devices e.g. spin valves & magnetic tunnel junctions

\[ H_E = -\frac{H_{C-} - H_{C+}}{2} \]

\[ H_E = \frac{J_{INT}}{M_{FM} t_{FM}} \]

\[ K_{AFM} t_{AFM} \geq J_{INT} \]
Exchange biasing of (Ga,Mn)As by MnO

- Exchange coupling of (Ga,Mn)As with MnO: bias in field cooled hysteresis loop + increased coercivity; no effect when zero field cooled.
- Sign of bias is reversed when cooling field is reversed.

\[ H_E = -\frac{H_{C-} - H_{C+}}{2} \]

\[ \Delta E = H_E t_{FM} M_{FM} \approx 3 \times 10^{-3} \text{ erg/cm}^2 \]
• **Curie temperature** ($T_C$) determined from temperature variation of remanent magnetization $M(T)$

• **Blocking temperature** ($T_B$) determined from temperature variation of exchange bias field $H_E(T)$

• Both cases are unconventional examples of exchange bias: $T_C < T_N$

• Note comparison with blocking temperature:
  • Upper panel: $T_C \sim T_B$
  • Lower panel: $T_C >> T_B$

4 nm MnO/10nm GaMnAs

$T_C = 55 \text{ K}$
$T_B = 48 \text{ K}$

8nm MnO/10nm GaMnAs

$T_C = 90 \text{ K}$
$T_B = 48 \text{ K}$
IV. Nanoengineered Curie Temperature in Laterally Patterned (Ga,Mn)As Heterostructures

With K. F. Eid, B. L. Sheu, O. Maksimov, M. B. Stone & P. Schiffer
Appl. Phys. Lett. 86, 152505 [2005]
Can annealing yield (Ga,Mn)As devices operating at $T >> 77$ K?

- Devices typically involve “buried” layers of (Ga,Mn)As [e.g. magnetic tunnel junctions]
- Early studies of annealing such devices showed no improvements in $T_C$

Nanoengineering of Defect Diffusion Pathways

Cap layer thicknesses as small as 7 monolayers completely suppress annealing enhanced $T_C$.

50 - 100 nm
Fabrication of (Ga,Mn)As nanowires using e-beam lithography & dry etching.
- Wire length 5 - 10 µm, widths 70 nm - 1µm
- Wire orientations along different principal crystalline axes: test for possible anisotropy
- Measure Curie temperature in single wire before and after annealing (at 180°C) using temperature dependent resistivity [peak in resistivity close to $T_C$]
Control measurements: unprocessed samples

- Peak in $\rho(T)$ closely correlated with $T_C$ as measured by $M(T)$.
- Unprocessed sample: $T_C \approx 60$ K both before and after annealing as expected from earlier studies.

Aside: origin of resistivity peak at $T_C$ still subject of debate (see e.g. Timm, Raikh, Oppen PRL 94, 036602 [2005])
Enhancement of $T_C$ in Nanowires

- 1µm width wire shows very slight increase ($\Delta T_C \sim 5 - 10$ K)
- 70 nm wires show large increase ($\Delta T_C \sim 40 - 60$ K)
- No observable dependence of defect diffusion on crystalline direction -- wires patterned along different crystalline axes show similar enhancements of $T_C$.

(Eid et al, APL [2005])
Dependence of $T_C$ on annealing time and on wire width

(B. L. Sheu et al, J. Appl. Phys. [2006])
Dependence of conductivity on annealing time and on wire width

- Variation of Curie temperature with annealing time & wire width correlates well with variation of conductivity.
- Can this be interpreted using simple diffusion models?
1D model for vertical outdiffusion of defects (e.g. Tuck (1974))


Assumption: change of conductivity entirely caused by increase in hole density

\[ \sigma(t) = \sigma_0 - \sigma_1 n(t) \]

\[ n(t) = \frac{N}{L} \frac{1}{\sqrt{4\pi Dt}} \int \int \exp \left[ -\frac{(x-x')^2}{4Dt} \right] dx dx' \]

\[ \frac{d\sigma}{dt} = f \left( \frac{t}{L^2} \right) \]
Data for lateral diffusion is inconsistent with naïve diffusion model
- Implies that diffusion constant decreases dramatically with wire width
- Caveat: conductivity determined by both hole density & mobility -- depletion effects + surface properties can modify mobility drastically
Outline

- Controlling spins in semiconductor heterostructures: overview
- Spin transport & scattering in (Ga,Mn)As devices:
  - Non-collinear spin valve effect in trilayer devices
  - Pinning and controlling domain walls at constrictions & interfaces
- Interfacial control of ferromagnetism in (Ga,Mn)As
  - Exchange biasing of (Ga,Mn)As by MnO (Eid et al., APL 85, 1556 [2004], Eid et al. J. Appl. Phys. 97, 10D304 [2005])
  - Nanoengineered $T_C$ in submicron (Ga,Mn)As wires (Eid et al, APL 86, 152505 [2005])